Contribution ID: **35** Type: **Oral Presentation**

#2-35 ANAQIN-X: A prototype low noise ASIC for the readout of highly dense semiconductor X-ray detectors

Thursday, June 12, 2025 11:20 AM (20 minutes)

IDeF-X (Imaging Detector Front-end in X-rays) is an integrated circuit family devoted to Read semiconductor detectors for space science application. Most of those circuits are based on one-dimensional analog channel (Strips). A new branch of 2-dimensional (pixels) IDeF-X has been designed to be able to reach ultra-low noise levels (D2R1 & D2R2). For this new branch, we have designed two previous pixelated integrated circuits with promising results. However, a high-level of noise has been spotted and yet to be explained. This article presents ANAQIN-X (Advanced Noise-optimized ASIC for Quantifying and Imaging in X-rays) the latest 2-Dimentionnal integrated circuit designed to investigate the origin of that noise. ANAQIN-X is dedicated to test different architectures of Charge Sensitive Amplifiers, the first stage of the spectroscopic signal processing analog circuit. The chip is designed to read out low leakage current (~ 20 pA), low capacitance (< 1 pF), X-rays photon counting (CdTe/CdZnTe/Si) detectors in order to perform high-resolution (500 eV FWHM at 60 keV) hard X-ray (1-220 keV) spectroscopy. Its main bloc is a mini matrix of pixels of 250 µm x 250 µm designed in X-FAB's 0.18-µm CMOS technology. Each channel consume 250 µW in nominal mode. It consists of a tunable gain Charge Sensitive Amplifier followed by a Pole-Zero Cancelation circuit operating as a CR-RC filter with a tunable peaking time (from 144 ns up to 3,6 µs) , and a peak detector. The different CSA architectures integrated on this chip are based on continuous reset nMOS and pMOS architectures with various W/L ratio of the input transistor. The chip include also, AC-coupled first stages with a tunable input capacitance (from 100 fF to 30 pF). A novel AC-coupling architecture has been developed, which involves integrating the coupling capacitor inside the feedback loop of the amplifier. This configuration allows a reduction in the thermal noise generated by the reset transistor and the usage of small value capacitance. An overall noise reduction of 10% at 10 pA of leakage current, and coupling capacitance of 1 pF is enough to get 98 % of gain according to the mathematical model. Simulation results have shown that with 300 fF detector connected to the input, the best performing pixel should be able to reach an Equivalent Noise Charge (ENC) of 18 el.rms. The circuit has been designed, is currently in production, and will be tested by January 2025. Space borne application requires a radiation hardness test to the Total Ionizing Dose (TID). An irradiation of the frontend electronics is planned using a 60Co gamma ray source by March 2025. The pixel showing the best noise performances will be selected and used in a "full-scale" (32x32 or 48x48 matrix) readout integrated circuit intended for an integration in MC2 (Mini CdTe on-Chip), a 4 sides connectable, compact, and fully digital counting X-rays photons imaging spectroscopy module designed for future space borne science applications.

Primary author: BOULFANI, Hani

Co-authors: Prof. MEURIS, Aline (DAP AIM, IRFU, CEA Saclay); Dr BAUDIN, David (DEDIP, IRFU, CEA, Paris Saclay University); Dr GEVIN, Olivier (DEDIP, IRFU, CEA, Paris Saclay University); Prof. LIMOUSIN, Olivier (DAP AIM, IRFU, CEA Saclay,)

Presenter: BOULFANI, Hani

Session Classification: #02 - Space Sciences and Technology

Track Classification: 02 Space Sciences and Technology