Contribution ID: **113** Type: **Poster**

#1-113 Simulation of Signal Reconstruction Algorithms in the ATLAS Tile Calorimeter PreProcessor for the HL-LHC

Tuesday, June 10, 2025 4:35 PM (5 minutes)

The Tile Calorimeter is a central sampling hadronic calorimeter of the ATLAS experiment at LHC. The calorimeter is build of alternating layers of stainless steel and plastic scintillating tiles oriented perpendicular to the beam axis. The calorimeter plays a crucial role in the reconstruction of jets and hadronically decaying tau leptons, as well as of the missing transverse energy. Moreover, it provides input signals to the Level 1 calorimeter trigger.

A new phase of the LHC, High-Luminosity LHC (HL-LHC), is expected to start its operation in 2030. The HL-LHC accelerator is designed to deliver five times the LHC nominal instantaneous luminosity. The demanding conditions in the detector during the HL-LHC operation, are driving significant upgrades to the ATLAS detector to enhance data processing and maintain its discovery potential. A crucial part of this upgrade is the replacement of the readout electronics for the ATLAS Tile Calorimeter.

The new Tile PreProcessor (TilePPr) system will serve as the interface between the calorimeter's on-detector electronics and the central Trigger, Detector Control, and Data Acquisition systems of ATLAS. Developed using the Advanced Telecommunications Computing Architecture (ATCA), the TilePPr module features high speed optical links and advanced data processing capabilities to ensure efficient handling of the increased data rates and harsher radiation environments characteristic of HL-LHC. One of the primary and most challenging functions of the TilePPr is to perform real time signal reconstruction, delivering calibrated data for each bunch crossing in a fixed and low latency path. Given the limited FPGA resources, reconstruction algorithms must be optimized for fixed-point arithmetic, reduced latency, and precise energy calculation for each bunch crossing, despite significant pile-up challenges.

To meet these demands, a dedicated framework has been developed to facilitate the design and assessment of various reconstruction algorithms within the TilePPr's FPGA architecture. This framework allows for in-depth evaluation using both simulated and real detector data to ensure the algorithms perform within the strict pile-up environment and timing constraints of the trigger system. This contribution will focus on the design, implementation and performance studies of various reconstruction algorithms within the TilePPr for the HL-LHC requirements.

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Session Classification: #01 - Fundamental Physics

Track Classification: 01 Fundamental Physics