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#1-98 The Compact Processing Module for the Upgrade of the ATLAS Tile Calorimeter Towards the High-Luminosity LHC

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The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN. In 2026, the LHC will undergo a series of upgrades leading to the High-Luminosity LHC (HL-LHC), which will provide an instantaneous luminosity 5 to 7 times larger than the nominal LHC design value. The ATLAS Tile Calorimeter Phase-II Upgrade (2026-2030) will completely replace the readout electronics with a new clock distribution and readout architecture with a fully digital trigger system to process more complex physics events while maintaining the trigger selection performance.

In the upgraded readout architecture, the on-detector readout electronics will transmit detector data to the Compact Processing Modules in the counting rooms for every bunch crossing (~25 ns). This new architecture will increase the data bandwidth required to read out the detector from the present 165 Gbps up to 40 Tbps. The Compact Processing Modules will transmit calibrated energy and time per cell to the first level of the ATLAS trigger system through the Trigger and DAQ interface system (TDAQi), as well as Level-0 selected data to the Front-End LInk eXchange (FELIX) system. In addition, the Compact Processing Modules will be responsible for distributing the LHC clock towards the on-detector electronics for the sampling of the PMT signals. A total of 128 CPMs, hosted in 32 ATCA carriers, will be required to read out the entire calorimeter during the HL-LHC data taking.

The communication with on-detector electronics is implemented using the GigaBit Transceiver (GBT) protocol with fixed and deterministic latency. Up to 32 uplinks running at 9.6 Gbps are required to read out detector and to monitor data from two TileCal modules, while the 16 downlinks at 4.8 Gbps are used to configure the on-detector electronics and distribute the bunch-crossing accelerator clock.

The energy per channel is reconstructed and calibrated in real-time for every bunch-crossing (~25 ns), and then transmitted to the TDAQi for the computation of complex trigger objects. In parallel, raw channel data and its associated reconstructed energy are stored in pipeline memories with a depth of 10 µs. Upon receiving a Level-0 trigger acceptance signal, the selected data is transmitted to the FELIX system through Full-Mode links at 9.6 Gbps. The CPM tracks and corrects with sub-nanosecond resolution phase drifts of the distributed clock to the on-detector electronics.

The CPM has been designed as a single Advanced Mezzanine Card (AMC) form factor equipped with six Samtec FireFly modules and a Xilinx Kintex UltraScale KU115 FPGA handling the readout, processing and configuration functionalities. A dedicated jitter cleaner is also included in the CPM to achieve synchronous communication between the on-detector electronics and subsequent levels of the ATLAS DAQ system. Each CPM can operate up to two TileCal modules via the Samtec FireFly modules and it provides seven high-speed interconnections through the ATCA carrier for the communication with the TDAQi. Two SFP modules located in the front panel enable the communication with the FELIX system for the transmission of triggered events. The complexity of the PCB design of the CPM and ATCA carrier required numerous signal and power integrity simulations. These simulations, performed using ANSYS electromagnetics, minimized impedance mismatch along the high-speed interconnections, and guided the selection of dielectric materials for controlling the signal attenuation.

This contribution describes in detail the design of hardware, firmware and software components of the Compact Processing Modules for the ATLAS Tile Calorimeter at the HL-LHC. Results from integration tests and

test beam campaigns are presented, as well as the commissioning of the CPM for the readout of the Tile Phase-II Upgrade Demonstrator module in the ATLAS experiment.

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