ANIMMA 2021 Conference in Prague

Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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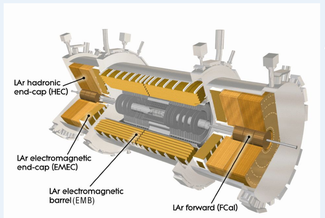
1. Introduction

HL-LHC Plan :

- High Luminosity Large Hadron Collider (HL-LHC) upgrade in 2025-27
- Instantaneous luminosity will increase by a factor of 5 to 7.5 with respect to nominal
- Planned integrated luminosity : up to 4000 fb^{-1} after 12 years

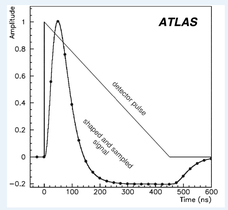


ATLAS LAr Calorimeter :

- Liquid Argon (LAr) based sampling calorimeter with lead (EM), copper (HEC) and both copper and tungsten (FCal) absorbers
- Incoming electrons, photons and hadrons shower in the absorber and ionize the Liquid Argon
- Triangular ionization signal amplified, shaped and sampled at 40 MHz
- 182,468 channels

New challenges at HL-LHC :

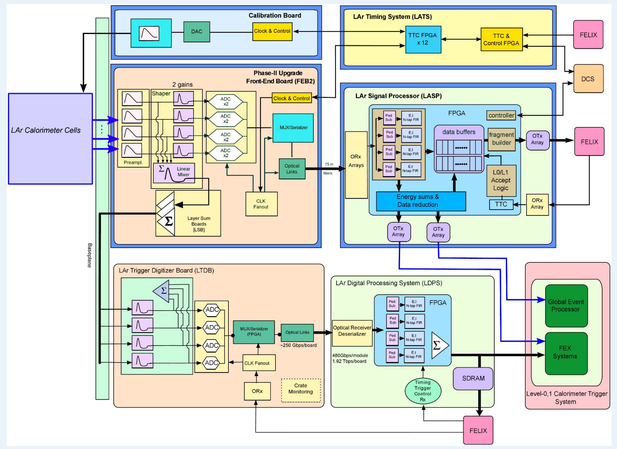
- Current readout electronics radiation tolerance : 700-1000 fb^{-1}
- Dramatic increase in number of interactions per bunch crossing :
  - From an average of around 35 to up to 200
  - Challenge for trigger to keep up with current performance
  - Increased “pileup” noise in trigger and readout electronics due to overlapping pulse shapes from minimum bias events



2. Upgrade Overview

Phase-I Upgrade [1] :

- New LAr Trigger Digitizer Board (LTDB) and LAr Digital Processing System (LDPS) installed during Long Shutdown 2 (LS2)
  - Staged hardware trigger upgrade to maintain trigger efficiency and bandwidth at at higher instantaneous luminosity
  - Accommodate for finer granularity and longitudinal information to be made available for hardware trigger



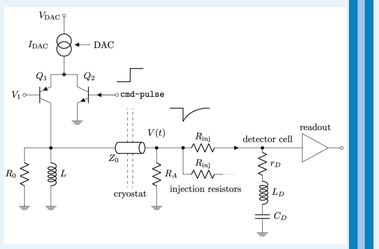
Phase-II Upgrade [2] :

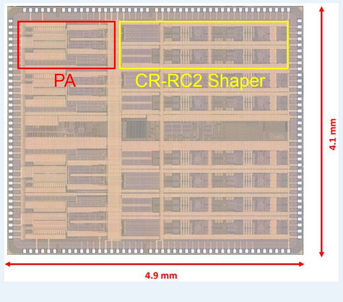
- Focus of poster : full upgrade of main readout chain (on-detector and off-detector electronics) during Long Shutdown 3 (LS3)
  - Provide full detector granularity to hardware trigger
  - Transmit all data off-detector at 40 MHz for processing
  - Radiation-hard front-end electronics

3. Front-End

Calibration System :

- **Requirements :**
  - 1 Calibration board : simulate ionization from energy deposits for 128 channels
  - Integral non-linearity (INL) <0.1%, pulse rise-time < 1 ns, uniformity <0.25% and radiation tolerant
  - Must cover full dynamic range : 320 mA, up to -7.5 V output : requires HV-CMOS
- **CLAROCv3 ASIC :**
  - 180 mm XFAB technology
  - Pulser with four high-frequency switches
- **LADOCv1 ASIC :**
  - 130 nm TSMC technology
  - 16-bit DAC with slow control chip configuration
  - 32 channel board in production



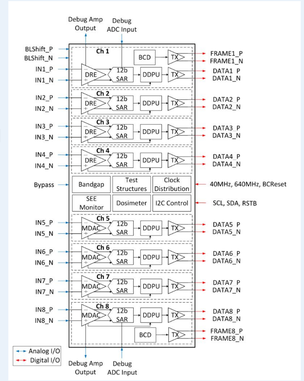


Preamplifier-Shaper ASIC :

- **Requirements :**
  - Analog processing : amplify and shape ionization pulses in two overlapping gain scales
  - 4 channel summing for hardware trigger
  - CR-RC^2 shaping
  - Large dynamic range : 10 mA for 25 Ω channels and 2 mA for 50 Ω channels
  - Noise : < 350 nA for 10 mA channels, <120 nA for 2 mA channels, INL < 0.2%
- **ALFE1 ASIC :**
  - 130nm CMOS TSMC, meets specifications
  - Tuneable input impedance and time constants
  - ALFE2 design with improvements submitted in April

Digitization :

- **Requirements :**
  - 40 MHz 8 channel Analog to Digital Converter (ADC)
  - 14-bit dynamic range with >11-bit precision
- **COLUTAv3 :**
  - Fully custom ASIC in 65 nm CMOS
  - Dynamic Range Enhancer (DRE) or Multiplying Digital to Analog converter (MDAC) + 12-bit Successive Approximation Register (SAR) ADC
  - Digital Data Processing Unit (DDPU) outputs data to optical links at 640 MHz
  - Achieves 11.7 and 11.3 Effective Number of Bits (ENOB) at 1 and 8 MHz respectively
  - INL < 0.04%, oE/E = 0.03%, cross-talk < 0.002%
  - COLUTAv4 to be submitted this summer



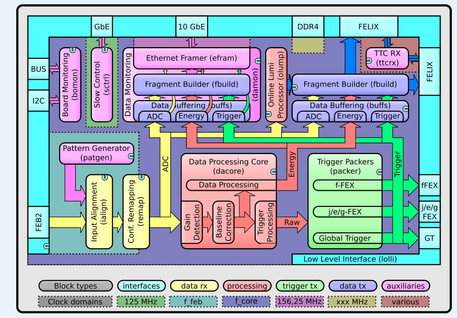
Front-End Board :

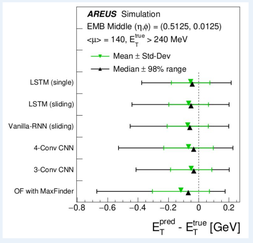
- **Requirements :**
  - Read out 128 channels per Front End Board (FEB)
  - Integrate PA/S, ADC and optical links
  - Provide clock, control, configuration and monitoring functions
  - Provide trigger sum to LTDB
- **FEB2 slice testboard :**
  - ¼ of final board
  - Integrates on-detector electronics for 32 channels
  - Full digital functionality, including slow control and monitoring and redundant bi-directional clock and control links
  - Functionality of full readout chain and multi-channel performance demonstrated
  - Current tests focused on analog performance

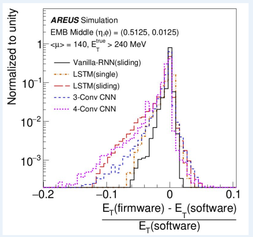
4. Back-End

LAr Signal Processing :

- **Requirements :**
  - Receive digitized waveform from 8 FEBs
  - Determine energy and timing of signals for up to 1024 channels
  - Provide energy sums and ordered cell energies above threshold for topological trigger algorithms
  - Output data, energy and timing at 25 Gbps for data acquisition
- **LASP Board :**
  - 2 Intel Stratix-10 Field Programmable Gate Arrays (FPGAs)
  - Fully functional test board design complete



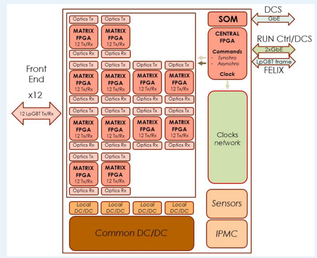




Machine Learning Studies :

- **Challenge :**
  - HL-LHC : up to 200 interactions per proton-proton bunch crossing
  - Pileup noise from overlapping of pulse shapes in consecutive bunch crossings will degrade energy, timing and trigger performance
- **Proposed Solution :**
  - Possibility of using advanced techniques such as machine learning algorithms in FPGAs for real-time energy reconstruction
  - Multiple algorithms show improved performance when compared to baseline Optimal Filter (OF) :
    - Convolutional Neural Networks (CNNs)
    - Long Short-Term Memory (LSTM) architectures
  - Both architectures have been successfully implemented and tested in FPGAs

Network	Frequency	Latency	Resource Usage			
	F_{max} [MHz]	clk_{core} cycles	#DSPs		#ALMs	
3-Conv CNN	493	62	46	0.8%	5684	0.6%
4-Conv CNN	480	58	42	0.7%	5702	0.6%
Vanilla-RNN (sliding)	641	206	34	0.6%	13115	1.4%
LSTM (single)	560	220	176	3.1%	18079	1.9%
LSTM (sliding)	517	363	738	12.8%	69892	7.5%



Timing System :

- **Requirements :**
  - Trigger, timing and control (TTC) for 1524 FEBs and 122 Calibration boards, 2 links per board
- **LATOURNET :**
  - One central and 12 “matrix” Cyclone10 GX FPGAs
  - v1 prototype board being designed

5. Summary and Outlook

- Both the on-detector and off-detector components of the ATLAS LAr calorimeter’s readout chain will be upgraded in time for the HL-LHC
- Custom ASICs for front end electronics have been designed and show promise to meet full specification requirements
  - Slice test board shows full digital and readout chain functionality
- Development of hardware and firmware components of back end electronics progressing
  - New processing algorithms show promise for coping with increased pileup at HL-LHC
- Phase-II upgrade on track for installation during LS3 despite pandemic

[1] CERN-LHCC-2013-017, [2] CERN-LHCC-2017-018