# Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

# Alessandro Ambler (McGill University) on behalf of the ATLAS Liquid Argon Calorimeter Group



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ATLAS LAr Electronics for the HL-LHC

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# The LAr Calorimeter at HL-LHC



High Luminosity Large Hadron Collider (HL-LHC) :

- Upgrade in 2025-27
- Instantaneous luminosity 5-7.5 times nominal
- Integrated luminosity up to 4000 fb<sup>-1</sup>
- Liquid Argon (LAr) Calorimeter :
  - Sampling calorimeter
  - Triangular ionization signal which is amplified, shaped and samples at 40 MHz
  - 182,468 channels
- New challenges for the LAr Calorimeter at HL-LHC :
  - Current front-end electronics radiation tolerance : 700-1000 fb<sup>-1</sup>
  - Average number of interactions per bunch crossing from 35 to up to 200
    - Challenge for trigger electronics as well as energy and timing measurements



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# Upgrade Overview

- Phase-II Upgrade :
  - Full upgrade of main readout chain
  - Provide full detector granularity to hardware trigger
  - Transmit all data off-detector at 40 MHz for processing
  - Radiation hard front-end electronics
- Front-End :
  - Custom ASICs in development for calibration system, preamplifier-shaper and digitization
    - Show promise to meet stringent requirements
  - Slice test board shows full digital and readout chain functionality
- Back-End :
  - Fully functioning test-board design for back-end digital signal processing
  - New energy reconstruction signal processing algorithms using machine learning techniques show promise



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# **Full Poster**

## ANIMMA 2021 Conference in Prague **Development of the ATLAS Liquid Argon Calorimeter** Readout Electronics for the HL-LHC

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## 1. Introduction



#### Phase-I Upgrade [1]

- New LAr Trigger Digitizer Board (LTDB) and LAr Digital Processing System (LDPS) installed during Long Shutdown 2 (LS2)
- Staged hardware trigger upgrade to maintain trigger efficiency and bandwidth at at higher instantaneous luminosity
- Accommodate for finer granularity and longitudinal information to be made available for hardware trioge



#### Phase-II Upgrade [2]:

- Focus of poster : full upgrade of main readout chain (on-detector and off-detector electronics) during Long Shutdown 3 (LS3)

- Provide full detector granularity to hardware trigger Transmit all data off-detector at 40 MHz for processing
- Radiation-hard front-end electronics

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# 3. Front-End

#### Calibration System :

#### Requirements :

- 1 Calibration board : simulate ionization from energy deposits for 128 channels
- Integral non-Energity (INI.) stil 1%, nuise rise-time < 1 ns, uniformity <0.25% and radiation tolerant
- Must cover full dynamic range : 320 mA, up to
- -7.5 V output : requires HV/CMOS

#### CLAROCV3 ASIC

- 180 mm XFAB technology
- Pulser with four high-frequency switches
- LADOCHLARK I

#### - 130 nm TSMC technolog

- 16-bit DAC with slow control chip configuration
- 32 channel board in production

### Preamplifier-Shaper ASIC :

- . Requirements Analog processing : amplify and shape ionization pulses in two overlapping gain scales 4 channel summing for hardware trigger STREET, STREET
  - CR-RC<sup>2</sup> shaping Large dynamic range : 10 mA for 25 Q channels and 2 mA for 50 Q channels Noise : < 350 nA for 10 mA channels, <120 nA for

m Q . w

- 2 mA channels. INL < 0.2% ALFE1 ASIC :
- 130nm CMOS TSMC meets specifications Tuneable input impedance and time constants

 ALFE2 design with improvements submitted in April 

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#### Digitization : Requirements :

- 40 MHz 8 channel Analog to Digital Converter (ADC) 14-bit dynamic range with >11-bit precision
- COLUTAV3 :
- Fully custom ASIC in 65 nm CMOS
- Dynamic Range Enhancer (DRE) or Multiplying Digital to Analog converter (MDAC) + 12-bit Successive Approximation Register (SAR) ADC
- Digital Data Processing Unit (DDPU) outputs data to
- Achieves 11.7 and 11.3 Effective Number of Bits
- INI < 0.04% oF/F = 0.03% cross-talk < 0.002%
- COLUTAv4 to be submitted this summer

### Front-End Board :

- nang to ang Requirements Read out 128 channels per Front End Board (FEB)
- Integrate PA/S. ADC and optical links
- Provide clock, control, configuration and
- Provide trigger sum to LTDB FFR2 slice testhoard
- Integrates on-detector electronics for 32
- Full digital functionality, including slow control and monitoring and redundant
- multi-channel performance demonstrated Current tests focused on analog
- nerformance
- ATLAS LAr Electronics for the HL-LHC

## 4. Back-End LAr Signal Processing :

- Requirements : Receive digitized waveform from 8
- FEBs Determine energy and timing of
- signals for up to 1024 channels Provide energy sums and ordered
- cell energies above threshold for
- Output data, energy and timing at 25 Gbos for data acquisition

#### LASP Board :

- 2 Intel Stratix-10 Field
- Programmable Gate Arrays
- Fully functional test board design

#### Machine Learning Studies :

- Challenge :
  HL-LHC : up to 200 interactions per proton-proton bunch crossing
  - Pileup noise from overlapping of pulse shapes in consecutive bunch crossings will degrade energy, timing and trigger performance

#### Proposed Solution :

- Possibility of using advanced techniques such as machine learning algorithms in FPGAs for real-time energy reconstruction
- Multinie algorithms show improved performance when compared to baseline Optimal Filter (OF) : - Convolutional Neural Networks (CNNs)
- Loon Short-Term Memory (LSTM) architectures Both architectures have been successfully implemented
- and tested in FPGAs

Network	Frequency	Lanecy	Revenue Usage			
	Fam (HRIC)	(Rue Odo	4052		843.96	
3-Cerv CNN	493	82	-46	4.8%	5684	6.6%
#Corr CNN	480	58	-42	0.7%	5702	8.6%
Vanilla 825N (shiftee)	641	206	34	4.6%	13115	1.0%
LSTM (similar)	550	230	176	215	19879	1.9%
LSTM (didno)	517	363	735	12.8%	69992	

### Timing System :

#### Requirements

- Trigger, timing and control (TTC) for 1524 FEBs and 122 Calibration boards. 2 links per board LATOURNET :
- One central and 12 "matrix" Cyclone10 GX FPGAs v1 prototype board being designed

## 5. Summary and Outlook

- Both the on-detector and off-detector components of the ATLAS LAr calorimeter's readout chain will be upgraded in time for the HL-LHC
- Custom ASICs for front end electronics have been designed and show promise to meet full specification requirements
- Sice test board shows full digital and readout chain functionality
- Development of hardware and firmware components of back end electronics progressing - New processing algorithms show promise for coping with increased pileup at HL-LHC
- Phase-II upgrade on track for installation during LS3 despite pandemic



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## optical links at 640 MHz