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#01-98 The Data Acquisition System for the ATLAS Phase-II Tile Calorimeter Demonstrator

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The Tile Calorimeter (TileCal) is the central hadronic calorimeter of the ATLAS detector at the Large Hadron Collider (LHC). This subdetector is a sampling calorimeter composed of steel plates as absorber material and plastic scintillators as active material. The complete readout of the detector is done using approximately 10,000 photomultipliers (PMTs).

The LHC will undergo a series of upgrades in 2025 leading to the High-Luminosity LHC (HL-LHC). The HL-LHC will provide an instantaneous luminosity 5 to 7 times larger than the nominal LHC design value. The ATLAS Tile Calorimeter Phase-II Upgrade (2025-2027) will completely replace the readout electronics with a new clock distribution and readout architecture with a full-digital trigger system.

In the upgraded data acquisition architecture, the on-detector readout electronics will transmit digitized signals from the PMTs for every bunch crossing (~25 ns) to the Tile PreProcessor (TilePPr) boards located in the counting rooms. The TilePPrs will store the detector data in pipeline memories until the reception of a trigger acceptance signal activating data transmission to the ATLAS Front End Link eXchange (FELIX) system. The new readout system will require 32 TilePPr modules to read out the entire detector for a total bandwidth of 40 Tbps. In parallel, the Trigger and Data Acquisition Interface boards will receive reconstructed cell energies from the TilePPrs and will transmit pre-processed trigger objects to the first level trigger with improved precision and granularity.

As part of the Phase-II Upgrade Demonstrator program, a full-size Demonstrator module containing all the upgraded readout electronics was installed into the ATLAS experiment in 2019 with the aim of validating the new clock and readout strategy for the Phase-II Upgrade.

The Demonstrator module consists of four independent mini-drawers capable to operate up to 12 PMT blocks. A mini-drawer is composed of a mechanical aluminum structure that supports one Mainboard, one Daughterboard, one high voltage regulation board, and up to 12 PMT blocks equipped with 3-in-1 cards. The PMT signals are shaped and amplified in two gains by the 3-in-1 cards and digitized in the Mainboard by 12-bit dual ADCs. The Daughterboards transfer the digitized data to the off-detector electronics through high-speed optical links. In addition, the lower gains of the 3-in-1 cards are summed in towers and transmitted to the Level-1 Calorimeter trigger system for trigger decision.

In the off-detector electronics, the Tile PreProcessor prototype receives the detector data for every bunch crossing through optical links with fixed and deterministic latency which provide a total data bandwidth of 160 Gbps. The main FPGA of the PreProcessor prototype processes and buffers the detector data in pipeline memories capable of storing up to 10 μ s of samples. Upon the reception of a trigger acceptance signal, the selected events are extracted from the pipeline memories, packed, and transmitted to the legacy Read-Out Drivers (RODs) keeping backward compatibility with the ATLAS DAQ system, and to the FELIX system.

The PreProcessor prototype also distributes the LHC bunch-crossing clock embedded with configuration commands to the on-detector electronics for synchronization with the accelerator. In the current Demonstrator, the Preprocessor prototype interfaces with the legacy Timing, Trigger and Control (TTC) system to receive the LHC clock and configuration commands. The recovered clock is then cleaned with dedicated jitter cleaner chips before driving it to the PreProcessor FPGA transceivers to ensure stable high-speed communication with the Daughterboards.

The Demonstrator module is fully integrated with the ATLAS TDAQ software and Detector Control System through the PreProcessor prototype, which translates the legacy commands into Phase-II commands, and transmits the triggered data to the RODs using the G-Link protocol. Therefore, the PreProcessor prototype enables the operation Demonstrator module for taking calibration and physics runs using the current ATLAS

software tools. From the point of view of the ATLAS TDAQ system, the Demonstrator module behaves as a legacy TileCal module.

The Demonstrator module has been operated together with the rest of the TileCal modules since its installation in June 2019. The performance of the upgrade electronics has been studied with Charge Injection, Laser, and Cosmic runs, showing excellent performance in terms of low noise, signal quality, and timing. One of the goals of the Demonstrator program is to keep the Demonstrator module in ATLAS during Run-3 (2021-2024) to continue studying its performance in real conditions.

This contribution describes in detail all the hardware, firmware, and software components of the clock distribution and data acquisition system for the Demonstrator module, focusing on the PreProcessor prototype developments, as well as the results of the Demonstrator module operation in the ATLAS experiment and future plans.

Primary author: CARRIÓ ARGOS, Fernando (Instituto de Fisica Corpuscular (CSIC-UV))

Co-authors: STAROVOITOV, Pavel (Ruprecht Karls Universitaet Heidelberg (DE)); ATLAS TILE CALORIMETER, Speakers Committee (CERN)

Presenter: CARRIÓ ARGOS, Fernando (Instituto de Fisica Corpuscular (CSIC-UV))

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